IN THE CLAIMS

Please amend and add claims as follows:

1. (Currently amended) A multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall substantially filled up with a plating layer having a substantially flat surface to form a viahole having a diameter; wherein:

the surface of said plating layer extends out of the through-holes and lies in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies;

at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm; and

the thickness of said conductor circuit layer is less than a half of the viahole diameter.

2. (Previously presented) The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall of the through-hole is roughened.

3. (Previously presented) The multilayer printed wiring board as set forth in Claim 1, wherein the plating layer surface and conductor circuit layer extending out of the through-holes are roughened.

4. (Canceled)

5. (Previously presented) The multilayer printed wiring board as set forth in Claim 1, wherein a further viahole is formed in the viahole.

6. (Previously presented) The multilayer printed wiring board as set forth in claim 1, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

7. (Previously presented) The multilayer printed wiring board as set forth in Claim 1, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

8. (Previously presented) The multilayer printed wiring board as set forth in Claim 1 , wherein the conductor circuit layer has a thickness less than 25 μm.

9. (Currently amended) The multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall substantially filled up with a plating layer having at least one surface to form a viahole having a diameter, wherein depressions are formed on a central surface portion of the plating layer surface extending out of the through-holes, and wherein the thickness of said conductor circuit layer is less than a half of the viahole diameter and less than 25 μm and wherein at least one of the surfaces of the

conductor circuits is roughened to a depth of 1 to 10 μm.

10. (Previously presented) The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall of the through-holes is roughened.

11.(Previously presented) The multilayer printed wiring board as set forth in Claim 9, wherein a depression is formed on a central surface portion of the plating layer surface extending out of the through-hole.

12. (Previously presented) The multilayer printed wiring board as set forth in Claim 9 , wherein the surface of the plating layer and the surface of the conductor circuit layer extending out of the through-holes are roughened.

13. (Canceled)

14. (Previously presented) The multilayer printed wiring board as set forth in Claim 9 , wherein a further viahole is formed in the viahole.

15. (Previously presented) The multilayer printed wiring board as set forth Claim 9, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

16. (Previously presented) The multilayer printed wiring board as set forth in Claim 9, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

17. (Currently amended) A multilayer printed wiring board comprising conductor

circuit layers each with at least one surface wherein at least one of the surfaces of the conductor circuit layer is roughened to a depth of 1 to 10 μm and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall wherein the inner wall is roughened, substantially filled up with a plating layer to form a viahole, wherein:

said roughened inner wall is covered with a roughened electroless plating layer; and

an inner space of said through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.

18. (Previously presented) The multilayer printed wiring board as set forth in Claim 17, wherein depressions are formed in the central surface portion of the plating layer surface extending out of the through-holes .

19. (Previously presented) The multilayer printed wiring board as set forth in Claim 17 , wherein the plating layer surface and conductor circuit surface extending out of the through-holes are roughened.

20. (Canceled)

21. (Previously presented) The multilayer printed wiring board as set forth in Claim 17, wherein a further viahole is formed in the viahole.

22. (Previously presented) The multilayer printed wiring board as set forth in any of Claims 17, wherein the interlaminar insulative resin layer in which the viaholes are

formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

23. (Previously presented) The multilayer printed wiring board as set forth in Claim 17 , wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

24. (Previously presented) The multilayer printed wiring board as set forth in Claim 17 , wherein the conductor circuit layer has a thickness less than 25 μm.

25. (Currently amended) A multilayer printed wiring board comprising conductor circuit layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall, substantially filled up with a plating layer to form a viahole, said interlaminar insulative resin layers being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

26. (Previously presented) The multilayer printed wiring board as set forth in Claim 25, wherein the interlaminar insulative resin layer is made of a composite of fluororesin fiber cloth, wherein said cloth comprises voids, and wherein a composite of thermosetting resin is impregnated in the voids in the cloth.

27. (Previously presented) The multilayer printed wiring board as set forth in Claim

25, wherein the inner wall of the through-hole is roughened.

28. (Previously presented) The multilayer printed wiring board as set forth in Claim 25, wherein depressions are formed in the central surface portion of the plating layer surface extending out of the through-holes.

29. (Previously presented) The multilayer printed wiring board as set forth in Claim 25 , wherein the plating layer surface and conductor circuit surface extending out of the hole for the through-holes are roughened.

30. (Previously presented) The multilayer printed wiring board as set forth Claim 25, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

31. (Previously presented) The multilayer printed wiring board as set forth in Claim 25 , wherein a further viahole is formed in the viahole.

32. (Previously presented) The multilayer printed wiring board as set forth in Claim 25 , wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

33. (Previously presented) The multilayer printed wiring board as set forth in Claim 25, wherein the conductor circuit layer has a thickness less than 25 μm.

34. (New) The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall is roughened, and the roughened inner wall is covered with a roughened

electroless plating layer, and an inner space of said through-holes defined by the electroless plating layer is filled up with an electroplating layer.

35. (New) The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall is roughened, and the roughened inner wall is covered with a roughened electroless plating layer, and an inner space of said through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.

36. (New) The multilayer printed wiring board as set forth in Claim 25, wherein the inner wall is roughened, and the roughened inner wall is covered with a roughened electroless plating layer, and an inner space of said through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.